AMENDMENT AND PRESENTATION OF CLAIMS

Please replace all prior claims in the present application with the following claims.

1. (Currently Amended) A circuit for a phase/frequency-locked loop comprising:

~~a phase/frequency comparator and~~

a frequency-generating oscillator[[,]]; and

a [[the]] phase/frequency comparator having two edge-triggered storage devices including a first edge-triggered storage device ~~which are respectively~~ set by an edge of a reference-frequency signal and a second edge-triggered storage device set by an edge of an output-frequency signal from the phase/frequency locked loop, ~~and which~~ the two edge-triggered storage devices are each reset by ~~an output~~ a resetting signal that is output from a resetting logic unit, the two edge-triggered storage devices have output signals that are connected to the frequency-generating oscillator, said resetting logic unit having ~~to whose~~ inputs that are supplied [[the]] with the output signals from the two edge-triggered storage devices,

wherein the ~~output~~ resetting signal from the resetting logic unit is only activated when both the output signals from the two edge-triggered storage devices have been activated, and is only de-activated when both the output signals from the two edge-triggered storage devices have been deactivated,

~~and in that~~ wherein the resetting logic unit ~~is implemented by means of~~ includes an asynchronous level-triggered RS storage device of inverse logic, the resetting input of the asynchronous level-triggered RS storage device having [[the]] an output signal from an OR gate supplied to it, and

~~in that~~ wherein the two edge-triggered storage devices each have only [[an]] a single output, the single output of each of the two edge-triggered storage devices being of non-inverted logic.

2. (Currently Amended) A circuit according to claim 1, wherein:

the output of the first edge-triggered storage device~~, to whose input the reference-frequency signal is applied~~ is fed to the frequency-generating oscillator to increase the frequency of the output-frequency signal, and the output of the second edge-triggered storage device~~, to whose input the output frequency signal, whose frequency may be divided if required, is applied~~ is fed to the frequency-generating oscillator to reduce the frequency of the output-frequency signal.

3. (Currently Amended) A circuit according to claim 1, wherein:

the output signals ~~at the outputs~~ of the two edge-triggered storage devices are connected to the frequency-generating oscillator via an interposed loop filter for stabilizing the phase-frequency-locked loop.

4. (Currently Amended) A circuit according to claim 1, wherein:

the frequency of the reference-frequency signal to the phase/frequency-locked loop is reduced by a factor N by ~~means of~~ a frequency divider ~~(2)~~, upstream of the input of the phase/frequency comparator.

5. (Currently Amended) A circuit according to claim 1, wherein:

the frequency of the output-frequency signal from the phase/frequency-locked loop is reduced by a factor M by ~~means of~~ a frequency divider, upstream of the input of the phase/frequency comparator.

6. (Currently Amended) A phase/frequency comparator for a phase/frequency-locked loop, comprising:

two edge-triggered storage devices including a first edge-triggered storage device ~~which are respectively~~ set by an edge of a reference-frequency signal for the phase/frequency-locked loop, and a second edge-triggered storage device set by an edge of an output-frequency signal from the phase/frequency-locked loop, ~~and which~~ the two edge-triggered storage devices are each reset by ~~an output~~ a resetting signal that is output from a resetting logic unit, said resetting logic unit having ~~to whose~~ inputs that are supplied [[the]] with the output signals from the two edge-triggered storage devices,

wherein the ~~output~~ resetting signal from the resetting logic unit is only activated when both the output signals from the two edge-triggered storage devices have been activated, and is only de-activated when both the output signals from the two edge-triggered storage devices have been deactivated, ~~and~~

wherein the resetting logic unit ~~is implemented by means of~~ includes an asynchronous level-triggered RS storage device of inverse logic, the resetting input of the asynchronous level-triggered RS storage device having [[the]] an output signal from an OR gate supplied to it, and

~~in that~~ wherein the two edge-triggered storage devices each have only [[an]] a single output, the single output of each of the two edge-triggered storage devices being of non-inverted logic.

7. (New) A circuit according to claim 2, wherein:

the output signals of the two edge-triggered storage devices are connected to the frequency-generating oscillator via an interposed loop filter for stabilizing the phase-frequency-locked loop.

8. (New) A circuit according to claim 2, wherein:

the frequency of the reference-frequency signal to the phase/frequency-locked loop is reduced by a factor N by a frequency divider, upstream of the input of the phase/frequency comparator.

9. (New) A circuit according to claim 2, wherein:

the frequency of the output-frequency signal from the phase/frequency-locked loop is reduced by a factor M by a frequency divider, upstream of the input of the phase/frequency comparator.

10. (New) A circuit according to claim 4, wherein:

the frequency of the output-frequency signal from the phase/frequency-locked loop is reduced by a factor M by a frequency divider, upstream of the input of the phase/frequency comparator.